Flash EEprom memory in a Flash EEprom system remain pending in this application.

The Examiner has rejected claims 63-67 under 35 U.S.C. Section 103 as being unpatentable under Furiya et al. in view of Terada et al.

Applicants respectfully disagree with the Examiner's contention that it is obvious to combine the cache memory as taught by Furiya et al with the EEPROMs of Terada.

Furiya et al. disclose and claim a cache memory incorporated into a magnetic disk controller for the purpose of improving magnetic disk access. Disk access performance is improved because the cache memory (RAMs) typically have much greater speeds (10^2 nanoseconds) compare to magnetic disks (10^7 nanoseconds.)

EEPROM and Flash EEPROM, being similar solid-state memory devices as RAMs, have similar speed as RAMs. There is no compelling motivation to use a RAM cache with an EEPROM or Flash EEPROM system.

On the other hand, as discussed in the specification as well as in previous communications, EEPROM and especially Flash EEPROM cannot be cycled through many write and erase operations. This has to do with the high voltage stress associated with write and erase operations intrinsic to these devices, as well as disturbance of one portion of the memory while another portion is being written. Thus, with use, defects tend to build up in the memory array and typically the devices are rendered unreliable after 10^3 to 10^4 write/erase cycles.

These devices are therefore conventionally used as semi-permanent storage of data, and the typical application is not expected to subject the devices to more than a few hundred write/erase cycles.

Applicants' claimed methods of extending the life of Flash EEprom memory in a Flash EEprom system employ a write cache to dramatically reduce the number of write (and therefore erase)

operations. In this way, it is possible to use a Flash EEprom system as a replacement for a magnetic disk storage, even though the expected number write/erase cycle may far exceed the cycling capacity of the Flash EEPROM devices.

Terada et al. merely disclose an improved read circuit for an EEPROM. There is no teaching of write cache nor the use thereof to reduce stress in an EEPROM or Flash EEPROM.

There is therefore no teaching or suggestion by Furiya or Terada, individually or in combination, of a method of extending the useful lifespan of EEPROM or Flash EEPROM system by reducing write-related stress with a write cache.

Claims 63-67 are now pending. In view of the Amendment and explanations given, reconsideration of the rejections is requested.

Entry of the foregoing is urged for the purpose of placing the application in condition for allowance or, alternatively, in better condition for consideration on appeal.

Respectfully submitted,

Philip Yau, Reg. No. 32,892

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MAJESTIC, PARSONS, SIEBERT & HSUE
Four Embarcadero Center, Suite 1450
San Francisco, CA 94111-4121
Telephone: (415) 362-5556
Facsimile: (415) 362-5418

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